Characterization of 4.5 kV Charge-Balanced SiC MOSFETs

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***Abstract*—This work demonstrates a novel charge-balanced (CB) silicon carbide (SiC) MOSFET that boasts a specific on-resistance of 10 mΩ·cm² at 4.5 kV breakdown voltage, surpassing the 1-D SiC unipolar limit. This is achieved through buried p-doped regions inside the drift layers, which are more easily scalable to higher voltages compared to the p-doped pillars used in super-junction (SJ) devices. Medium-voltage CB SiC MOSFETs with different p-doped bus widths and pitches have been fabricated and characterized in this work. The unique microstructure of these devices causes interesting macro-scale characteristics, such as distinctive steps in the capacitance–voltage curves and a turn-on voltage tail that reduces with increased temperature. The switching energy of the CB MOSFET is 92% lower than that of an IGBT at 150 °C. This paper presents and interprets these intriguing static and dynamic characteristics.**

***Keywords*—Charge-balanced MOSFET, SiC, characterization, capacitance steps, voltage tail**

I. Introduction

Silicon (Si) IGBTs are widely used in medium-voltage (MV) systems due to their low on-state losses at higher voltages; however, their bipolar structure causes slower switching speeds, resulting in high switching losses, and limited switching frequency [1]. At low frequencies, the volume and weight of passive components, such as filters and transformers, limit design flexibility and increase fabrication and installation costs for MV systems. Unipolar Si devices (e.g., MOSFET) have faster switching speeds than their bipolar Si counterparts, but their high conduction losses make them less suitable for MV applications than Si IGBTs [2-4].

Unipolar silicon carbide (SiC) devices can achieve lower on-resistance at higher voltages than unipolar Si devices thanks to the higher breakdown electric field strength and wider bandgap of the material. However, at MV (greater than 3.3 kV), it is still difficult for SiC unipolar devices (e.g., MOSFET) to compete with the low conduction losses of Si bipolar devices (e.g., IGBT) [2-4]. Accordingly, researchers have explored super-junction (SJ) structures to break this 1-D SiC limit (Fig. 1) [5-8]. However, applying the SJ structure to SiC requires complex fabrication processes, which become more challenging as the drift layer thickness increases, thereby limiting the voltage scaling. The charge-balanced (CB) structure addresses this issue by using buried p-doped regions in the drift layer (Fig. 2), which simplifies the fabrication and enables scaling to thicker drift layers and hence higher voltages [9-10]. To avoid floating CB-regions inside the drift layer, intermittent vertical p-type pillars (p-bus) were used throughout the active area to provide a conductive path for holes during turn on. In this work, four types of CB SiC MOSFETs with greater than 3.5 kV breakdown voltage were fabricated and characterized to assess the influence of the p-bus width and pitch on the device performance (Fig. 3).

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DEAR0000674 advised by Program Director Isik Kizilyalli. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof. The authors acknowledge the financial support provided by the U.S. Department of Energy Advanced Manufacturing Office through the Wide Bandgap Generation (WBGen) Fellowship at the Center for Power Electronics Systems (CPES) at Virginia Tech (http://www.eng.vt.edu/WBGen). This work was supported by the High Density Integration (HDI) mini-consortium of the Center for Power Electronics Systems (CPES) at Virginia Tech.

II. Static Characterization

A Keysight B1505A curve tracer was used to characterize the CB SiC MOSFETs. A power resistor and a ceramic

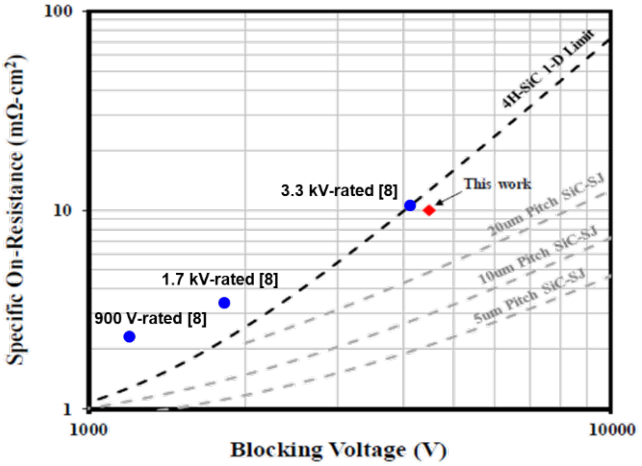
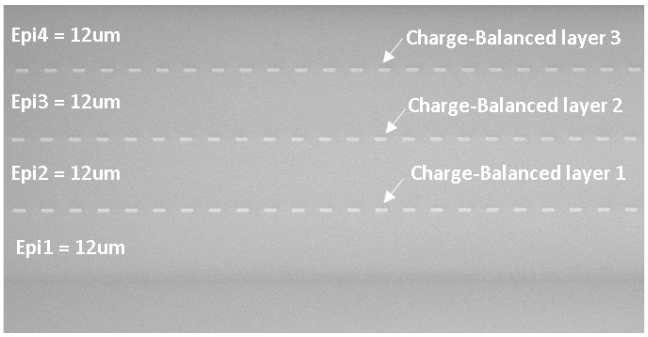
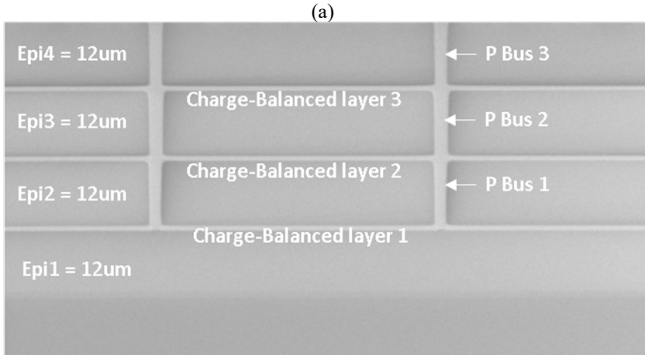


Fig. 1. Specific on-resistance vs. breakdown voltage limits for 1-D SiC unipolar devices (black curve and blue markers), SiC SJ devices (grey curves), and the experimental achievements from this work (red marker).

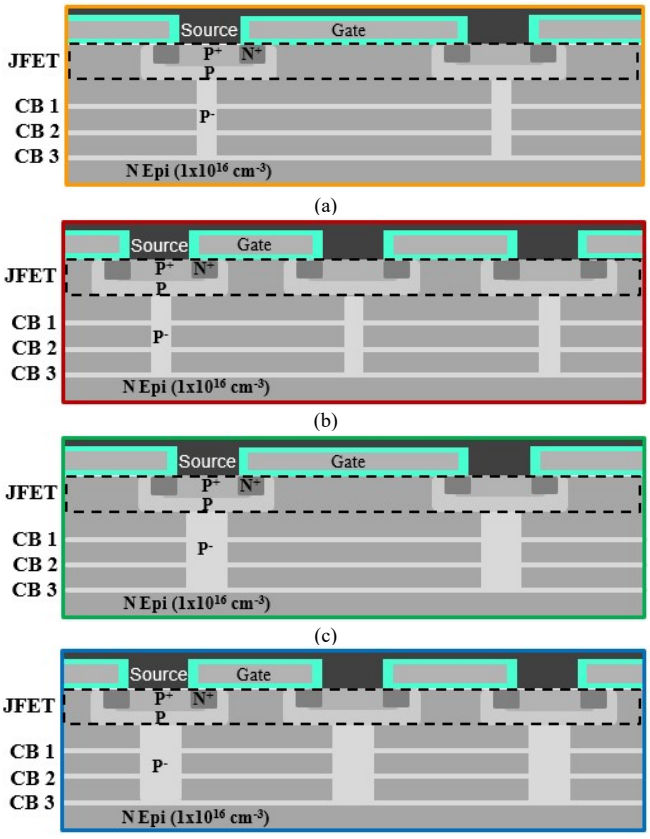


(a)



(b)

Fig. 2. SEM of the drift layer cross-section (a) parallel and (b) perpendicular to the CB SiC MOSFET gate fingers.



(a)

(b)

(c)

(d)

Fig. 3. Not-to-scale pictorial representations of the (a) narrow bus, large pitch (Type NL), (b) narrow bus, small pitch (Type NS), (c) wide bus, large pitch (Type WL), and (d) wide bus, small pitch (Type WS) bus designs.

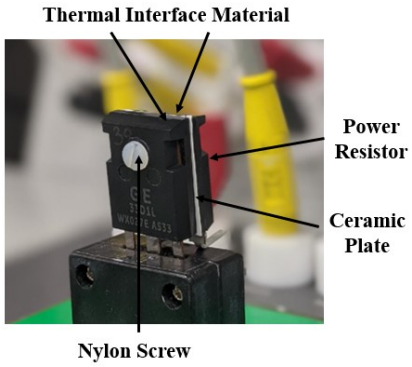


Fig. 4. Power resistor and ceramic isolating plate setup used to heat the CB MOSFETs.

isolating plate were clamped to the CB MOSFETs (Fig. 4) to heat them to the desired temperature during static characterization. A thermocouple was placed between the ceramic isolating plate and the device under test to get an approximate measurement of the junction temperature.

A. On-Resistance, Breakdown Voltage, Leakage Current, and Threshold Voltages

Fig. 5 shows the on-resistance vs. drain current at 25 °C and 175 °C for each device type. The devices with the wide and large pitch bus design (WL) have the lowest on-resistance, while the devices with the wide and small pitch bus design (WS) have the highest on-resistance. The p-type material added to the drift-layer decreases the available active area responsible for creating a conductive path when the CB MOSFETs are on; therefore, increasing the amount of p-type material in the drift layer – either by increasing the width of the bus or decreasing the pitch – will result in an increase in on-resistance.

Fig. 6 shows the breakdown voltages and leakage currents for each device type at room temperature. The breakdown voltage of all device types is greater than 3.3 kV. The type NL and WL devices have a different edge termination than the type NS and WS devices, which may affect their breakdown

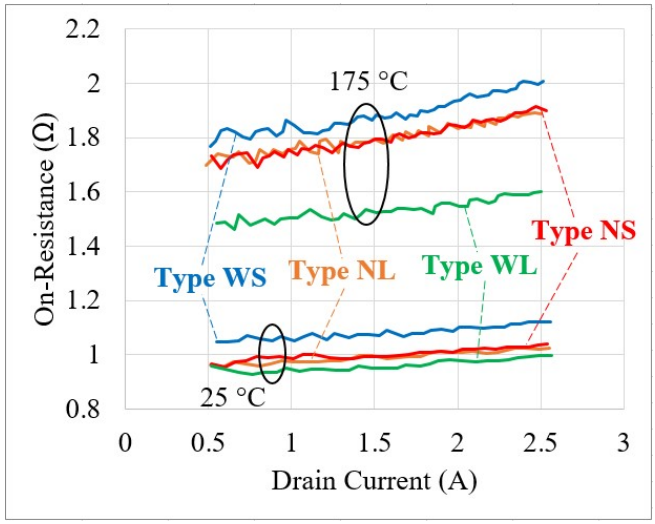


Fig. 5. On-resistance versus drain current at a gate-source voltage of 20 V for each device type.

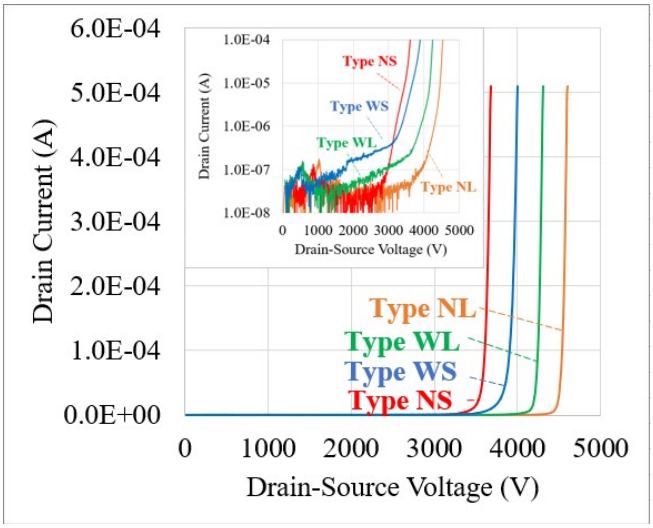


Fig. 6. Breakdown voltage and leakage current (inset) for all device types.

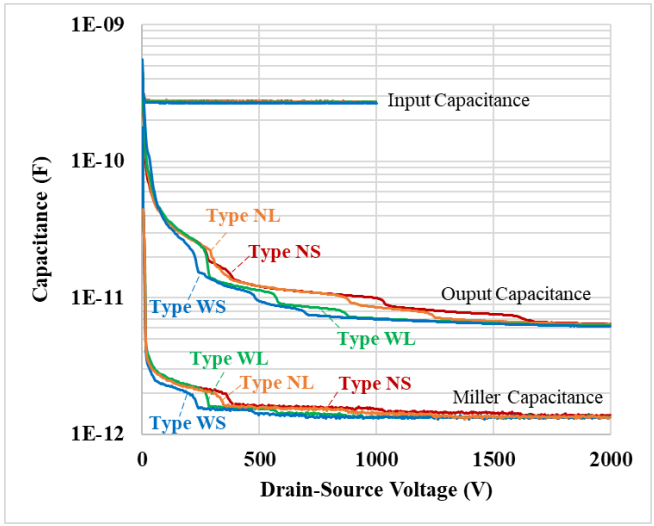


Fig. 7. Input, output, and Miller capacitances across drain to source voltage for all device types collected at a gate-source voltage of 0 V, a frequency of 1 MHz, and an AC voltage of 25 mV.

voltages. The devices with a narrow bus (NS and NL) show lower leakage current than their wide bus counterparts (WS and WL) with the same pitch. The high energy implantation process used to create the p-bus can damage the crystallographic structure of the drift layer, leading to higher leakage in wide bus devices.

The threshold voltages for each device type at room temperature and 175 °C are listed in Table I. They were extracted from the transfer characteristic curves using the constant current method by setting the gate-to-source voltage equal to the drain-to-source voltage to guarantee the device is operating in the saturation regime and measuring the gate voltage at a drain current of 1 mA [11].

B. Input, Output, and Miller Capacitances

The input, output, and Miller capacitances across drain to source voltage for all device types are plotted in Fig. 7. At 2 kV, the input, output, and Miller capacitances are 275 pF, 6.4 pF, and 1.4 pF, respectively. The output and Miller capacitances' relationships with drain to source voltage (Fig. 7) are of particular interest due to the unique steps seen in their waveforms. The cause of a similar singular step seen in the output capacitance of SJ MOSFETs has been identified [12] and its contribution to harmonic generation has also been studied [13]. The output and Miller capacitance steps in CB MOSFETs are caused by a rapid increase in depletion width as the individual depletion boundaries in the n-epi surrounding a single JFET or CB region meet. The steps occur at different voltages and have different heights because the contribution of the p-bus to the depletion of the n-epi varies with the distance from the source. The lowest voltage step is caused by the JFET region (Fig. 3), while the second, third, and fourth lowest voltage steps are caused by the CB region closest, second closest, and farthest from the source (Fig. 3), respectively (Fig. 8). The width and pitch of the p-bus is proportional to its contribution to the depletion of the n-epi. This causes the capacitance steps of wider and smaller pitch bus designs to occur at lower voltages (Fig. 8).

TABLE I. THRESHOLD VOLTAGES FOR EACH DEVICE TYPE AT 25 °C AND 175 °C

Device Type	Threshold Voltages	
	25 °C	*175 °C*
NL	3.77 V	2.95 V
NS	3.70 V	2.92 V
WL	3.76 V	3.06 V
WS	3.76 V	2.99 V

III. DYNAMIC CHARACTERIZATION

A double-pulse inductive switching test (DPT) was used to evaluate the dynamic performance of the CB SiC MOSFETs up to 3 kV (Fig. 9). Two 3.3 kV SiC Schottky diodes were used in series to freewheel the current for the 10 mH inductive load. The gate driving voltages were +20 V in the on-state and –5 V in the off-state. A low-inductance current shunt was used to measure the MOSFET drain current, a low-voltage passive probe was used to measure the gate-source voltage, and a high-voltage differential probe with up to 100 MHz bandwidth was used to measure the drain-source voltage (Fig. 9).

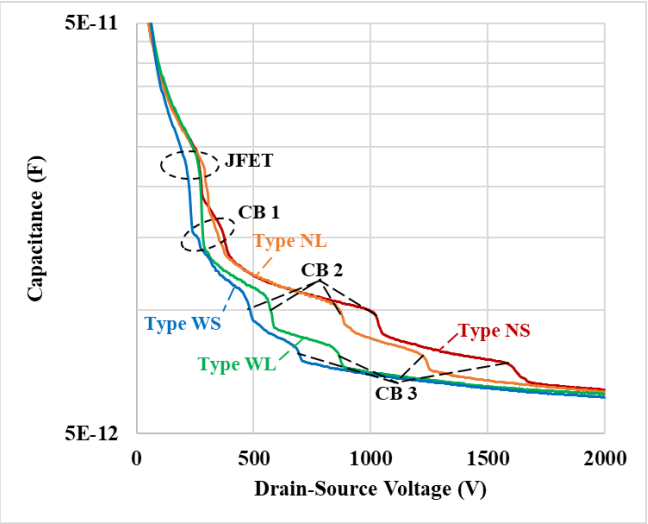


Fig. 8. Output capacitance steps associated with the JFET and CB regions.

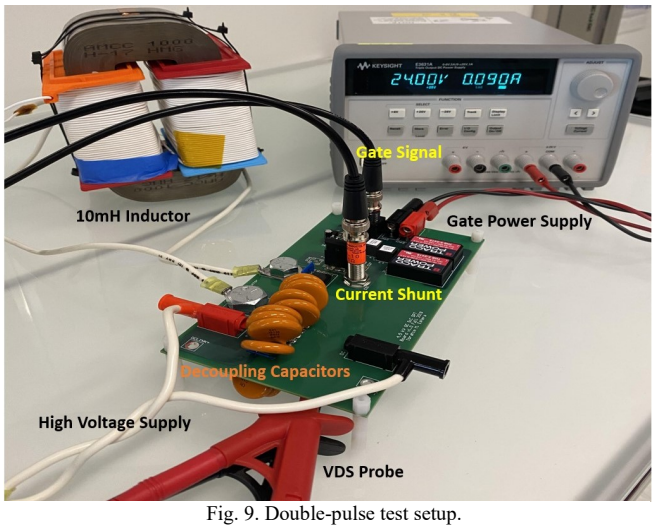


Fig. 9. Double-pulse test setup.

Fig. 10a and Fig. 10b show the DPT waveforms for the two device types with the highest and lowest voltage tails at 3 kV, 2 A and at temperatures of 25 °C, 100 °C, and 175 °C. The NL device has a voltage tail longer than 3.5 µs at 175 °C (Fig. 10a). The NS and WL devices (waveforms not included here) saw a reduction in their voltage tails from greater than 3.5 µs at room temperature to less than 1 µs at 175 °C. The WS device had the shortest voltage tail at room temperature and has negligible tail length at 175 °C (Fig. 10b).

Fig. 10c shows the DPT waveforms for all four of the CB SiC MOSFET device types at 3 kV, 2 A, and 175 °C. The NL device experiences a small rise in the drain-source voltage during the first on pulse, and a voltage tail at the second turn-on transient that exceeds 3 µs. The NS, WL, and WS devices had no measurable drain-source voltage rise during the first on pulse, and a shorter voltage tail (less than 1 µs) at the second turn-on transient. The voltage fall times decrease with a wider bus or a smaller pitch, indicating that an increase in total p-bus improves the dynamic performance.

The bump in the drain-source voltage seen during the first on period, and the drain-source voltage tail seen during the second on period (Fig. 10a) have the same physical explanation. The resistivity of SiC doped heavily with Al is at its highest point at low temperatures and begins to decrease as temperature increases [14]. The Al-doped p-bus pillars and p-type CB layers, therefore, have a higher resistance at lower temperatures. The higher the resistance of the p-bus pillars and CB layers, the longer it takes for a sufficient number of holes to reach the CB layers to eliminate the depletion region after turn on. The slow reduction of the depletion region in the n-type portion of the drift layer surrounding the CB layers creates a p-bus structure-, temperature-, blocking voltage-, and time-dependent variable on-resistance contribution from these regions. Since the current is still ramping up during the first on period, the induced on-state drain to source voltage caused by the high on-resistance is less obvious than during the second period. The on-resistance contribution of the depletion regions is not accounted for by the static on-resistance measurement (Fig. 5) because the devices were not subjected to a high

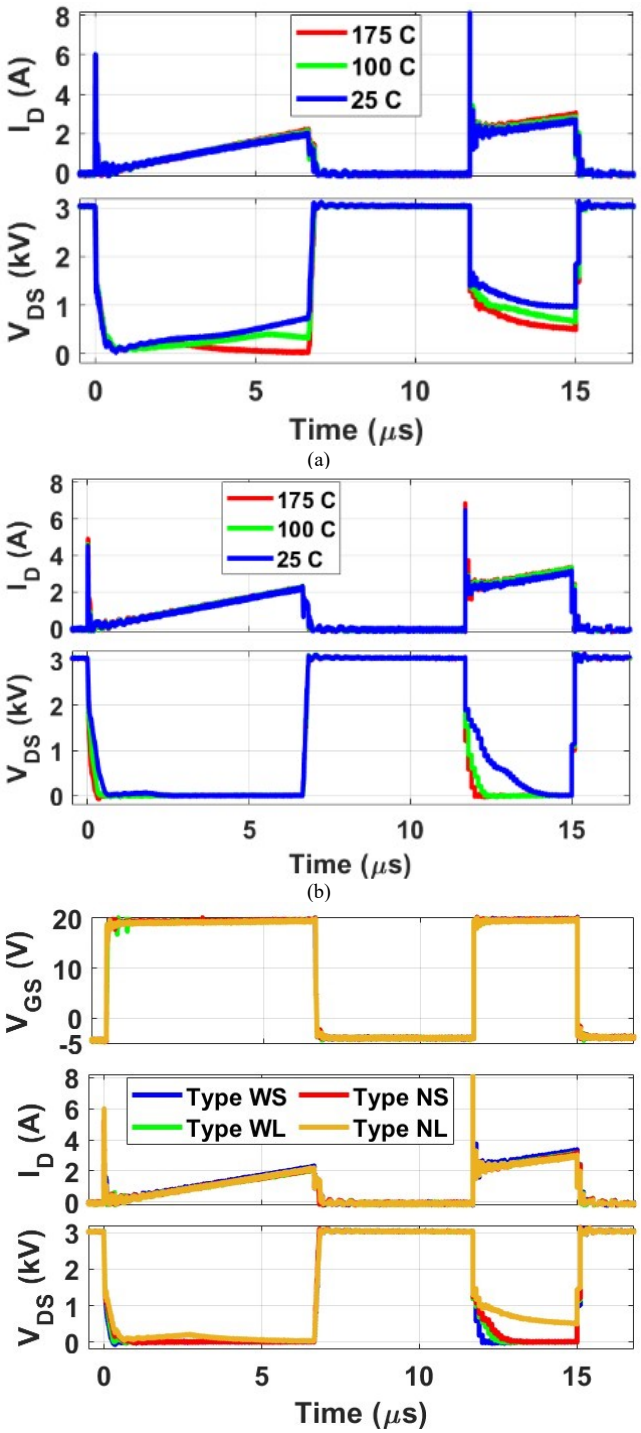
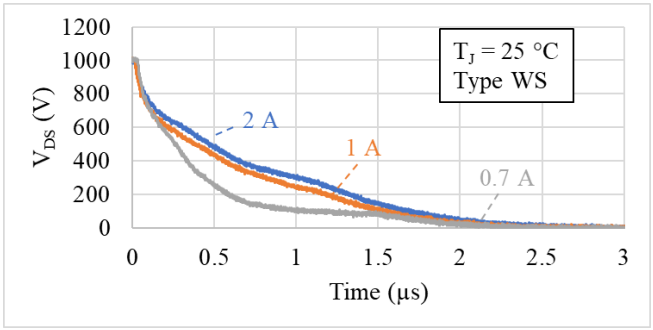


Fig. 10. Switching waveforms at 25 °C, 100 °C, and 175 °C for device types (a) NL and (b) WS. (c) Switching waveforms at 175 °C for the four different device types.

blocking voltage that would have generated a depletion region prior to measurement.

Differences in the drain-source voltage waveforms of the four device types during the on periods are also related to this principle. The device types with a narrower pitch and/or a



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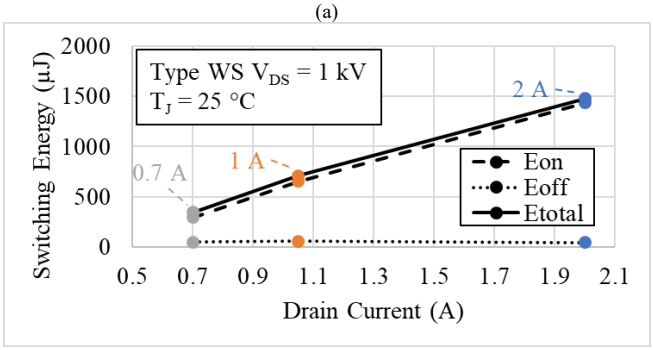

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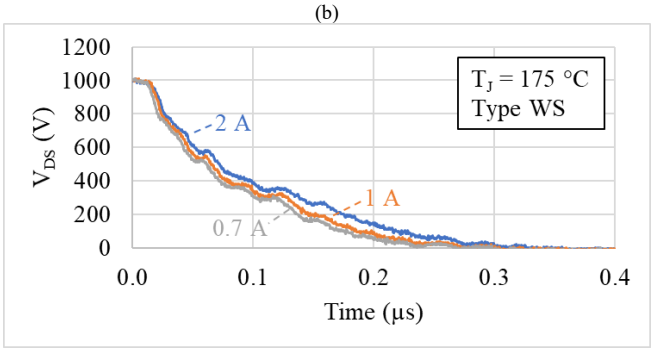

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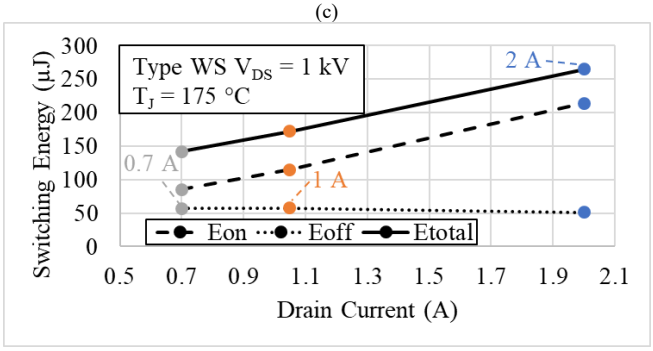
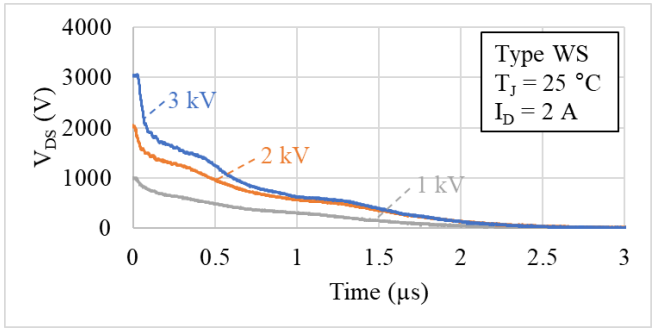


(d)

Fig. 11. (a) Drain to source voltages and (b) switching losses of a WS CB MOSFET at room temperature, 1 kV blocking voltage, 20 Ω gate resistance, and drain currents of 0.7 A, 1 A, and 2A. (c) Drain to source voltages and (d) switching losses of a WS CB MOSFET at 175 °C, 1 kV blocking voltage, 20 Ω gate resistance, and drain currents of 0.7 A, 1 A, and 2A.



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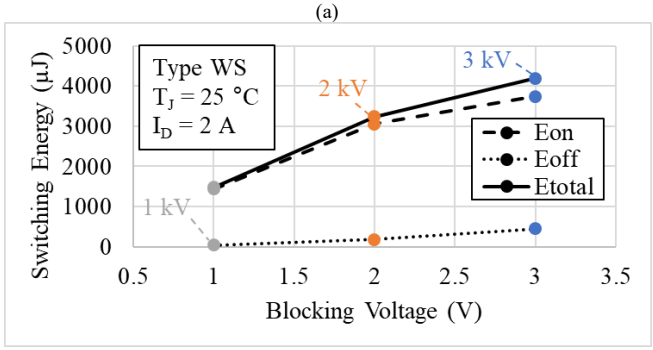

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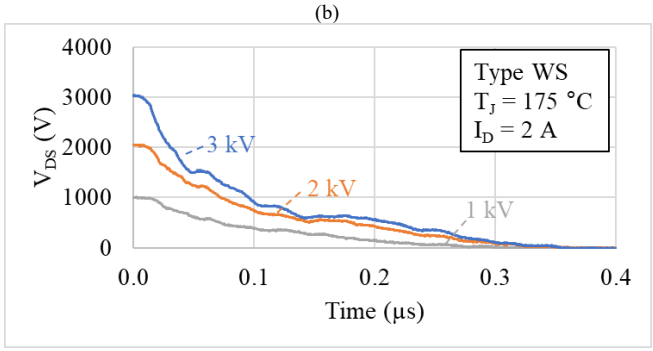

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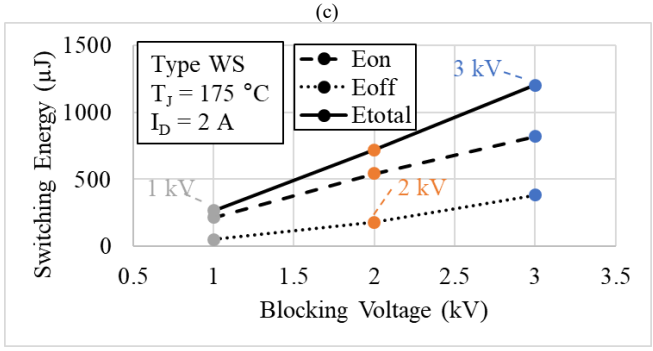


(d)

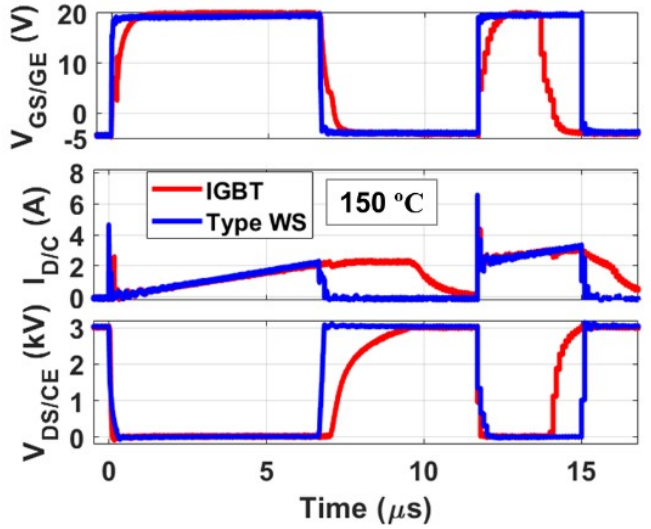
Fig. 12. (a) Drain to source voltages and (b) switching losses of a WS CB MOSFET at room temperature, 2 A drain current, 20 Ω gate resistance, and blocking voltages of 1 kV, 2 kV, and 3 kV. (c) Drain to source voltages and (d) switching losses of a WS CB MOSFET at 175 °C, 2 A drain current, 20 Ω gate resistance, and blocking voltages of 1 kV, 2 kV, and 3 kV.

wider bus have a larger conduction path for holes to reach the CB layers and, therefore, have a lower drain to source voltage tail. The effect of this is that, despite having a higher static on-resistance, the effective on-resistance of the devices with a narrower pitch and/or a wider bus is lower.

The drain to source voltage tails and switching energies for a WS device at room temperature, a drain to source voltage of 1 kV, and a 0.7 A, 1 A, and 2 A drain current are plotted in Fig. 11a and Fig. 11b, respectively. The linear increase in switching energy with drain current (Fig. 11b) indicates that the drain current does not induce a change in the variable on-

resistance, but simply induces a larger voltage drop across the existing variable on-resistance. A similar relationship is found in the drain to source voltage tails and switching energies for a WS device at 175 °C, a drain to source voltage of 1 kV, and a 0.7 A, 1 A, and 2 A drain current plotted in Fig. 11c and Fig. 11d, respectively. The consistency across temperature reinforces the conclusion that the drain current does not induce a change in the variable on-resistance.

The drain to source voltage tails and switching energies for a WS device at room temperature, a drain current of 2 A, and a 1 kV, 2 kV, and 3 kV drain to source voltage are plotted in Fig. 12a and Fig. 12b, respectively. The nonlinear increase in switching energy with blocking voltage (Fig. 12b) indicates that the blocking voltage contributes to the variable on-resistance non-linearly. The n-epi directly surrounding each individual CB layer depletes at less than 2 kV (as indicated by the output capacitance curves in Fig. 7b), contributing a higher variable on resistance at turn on than the n-epi farther from the CB layers that depletes at higher voltages. Although depleted n-epi has the same resistivity no matter where it is, the n-epi directly surrounding each individual CB layer has a lower cross-sectional area, causing the variable resistance contribution to be higher. The nonlinear relationship between blocking voltage and switching energy at room temperature erodes at higher temperatures (Fig. 12c and Fig. 12d). At higher temperatures, holes are transported more quickly to the CB layers, causing the n-epi to become un-depleted fast enough that the uneven contribution to the variable on-resistance can no longer be detected.



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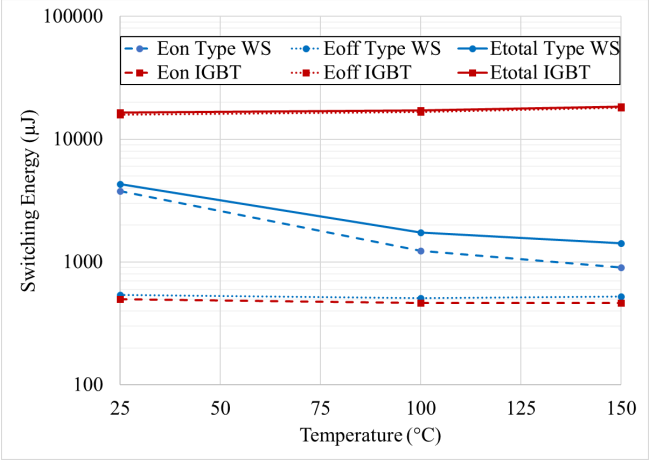

(b)

Fig. 13. (a) Switching waveforms at 150 ºC and (b) switching losses of a Si IGBT (red) and WS CB MOSFET (blue) at 3 kV drain to source voltage, 2 A drain current, and 20 Ω gate resistance.

Fig. 13a shows the DPT waveforms for a 4.5 kV Si IGBT (IXYX40N450HV) and a WS CB MOSFET at 3 kV, 2 A, and 150 °C. The switching losses versus temperature for the Si IGBT and the WS CB MOSFET are shown in Fig. 13b. The CB SiC MOSFET has 44% lower switching losses at 25 °C, and 92% lower losses at 150 °C, than the Si IGBT.

IV. Conclusion

The CB SiC MOSFETs evaluated in this work offer lower conduction loss than 1-D SiC unipolar devices, boasting a specific on-resistance of 10 mΩ·cm^2 at 4.5 kV breakdown voltage. They also offer 92% lower switching loss than Si IGBTs at 150 °C. Additionally, the CB structure is easier to manufacture, and more easily scaled to higher voltages than SJ pillars. Steps in the output and Miller capacitances of CB MOSFETs are dependent on p-bus design. The drain-source voltage of the CB MOSFETs after turn on is determined by the width and pitch of the buried p-buses. Operating the CB MOSFETs at higher temperatures reduces the voltage fall time by nearly four times. CB MOSFETs have the potential to push the boundaries of SiC into higher power applications.

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